UNIVERSITY OF BIRMINGHAM

eRD18 - Precision Central Silicon Tracking & Vertexing for the EIC

FY20 Report

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Proposal

To develop a detailed concept for a central silicon vertex detector for a future EIC experiment, exploring the potential advantages of depleted MAPS (DMAPS) technologies

Science drivers

Open heavy flavour decays – **high position resolution**

Precision tracking of high Q^2 scattered electrons – **low mass**

WP1: Sensor Development

Exploit on-going R&D in Birmingham into depleted MAPS to investigate potential solutions for the EIC

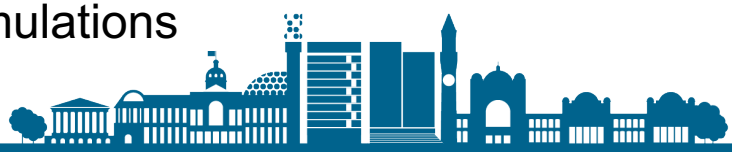
WP2: Silicon Detector Layout Investigations

Performance requirements: numbers of layers, layout and spatial resolution of the pixel hits

Work packages status

- **WP1: Sensor development**
  - **Technology investigations** on the TJ 180nm modified process: completed
    - Summary submitted to the panel in July last year
    - Mini-MALTA results included in latest report and published at https://doi.org/10.1016/j.nima.2019.163381
  - **Feasibility study** into an EIC specific DMAPS sensor: ongoing
    - Covered in this talk

- **WP2: Silicon Detector Layout Investigations**
  - **Basic layout simulations** based on EICRoot: completed
    - Baseline performance plots for a Si+TPC and all silicon tracker design
    - Report is being finalised
  - **Physics performance** simulations: ready to start
    - G4E framework installed and running (thanks for Yulia & Dmitry)
    - Ready to start heavy flavour physics simulations



EIC specific DMAPS sensor - Feasibility study

- The main focus of WP1 at present is a feasibility study into the design of an EIC specific DMAPS sensor, carried out in collaboration with a chip designer at RAL

- Aim: investigate options for the **pixel design and readout architecture** that would match the requirements for a tracking and vertex detector at an EIC, with the added capability to time stamp individual bunch crossings
  - The study tries to find solutions to design one DMAPS sensor that could be used both for vertex and tracking, and time stamping

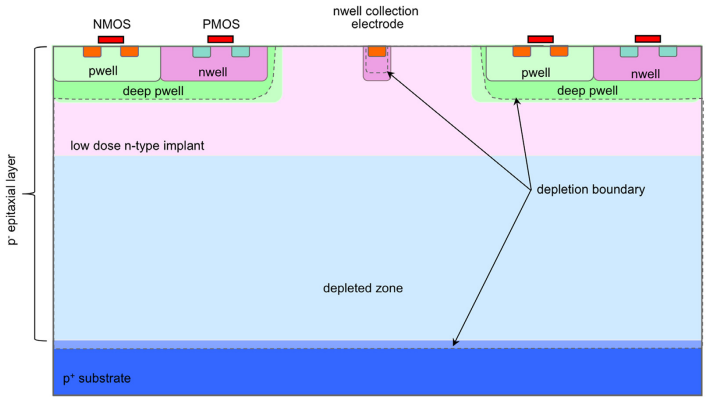
- The first part of the study on the pixel design has been completed

EIC specific DMAPS sensor - Specifications

- Aim for improved spatial resolution with respect to ALPIDE
  - Smaller pixels (20 x 20 μm^2)
  - Low mass detector layers (< 0.3% X/X_0 - low power)
- Consider readout requirements for the EIC
  - Integration time and time-stamping capability

	EIC DMAPS Sensor	
Detector	Vertex and Tracking	Added time stamping
Technology	TJ or similar	
Substrate Resistivity [kohm cm]	1	
Collection Electrode	Small	
Detector Capacitance [fF]	<5	
Chip size [cm x cm]	Full reticule	
Pixel size [µm x µm]	20 x 20	max 350 x 350
Integration Time [ns]	2000	
Timing Resolution [ns]	*OPTIONAL* *< 9 (eRHIC)* *< 1 (JLEIC)*	< 9 (eRHIC) < 1 (JLEIC)
Particle Rate [kHz/mm^2]	**TBD**	
Readout Architecture	Asynchronous	**TBD**
Power [mW/cm^2]	<35	<200
NIEL [1MeV neq/cm^2]	10^{10}	
TID [Mrad]	< 10	
Noise [electrons]	< 50	
Fake Hit Rate [hits/s]	< 10^{-5}/evt/pix	
Interface Requirements	**TBD**	

TJ 180 nm modified CIS process



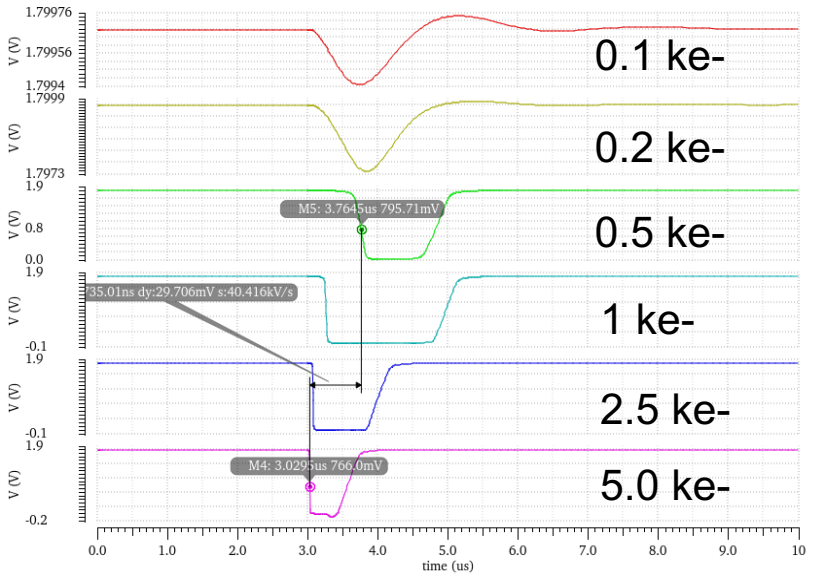
W. Snoeys et al,
http://dx.doi.org/10.1016/j.nima.2017.07.046

Time-walk

- **Time-walk** and **jitter** due to noise limit the timing performance of **traditional (pre-amp + comparator) pixel FE** architectures

- A simulation of the reproduced ALPIDE model shows a time-walk of 700 ns for charges between 0.5 and 5 ke-

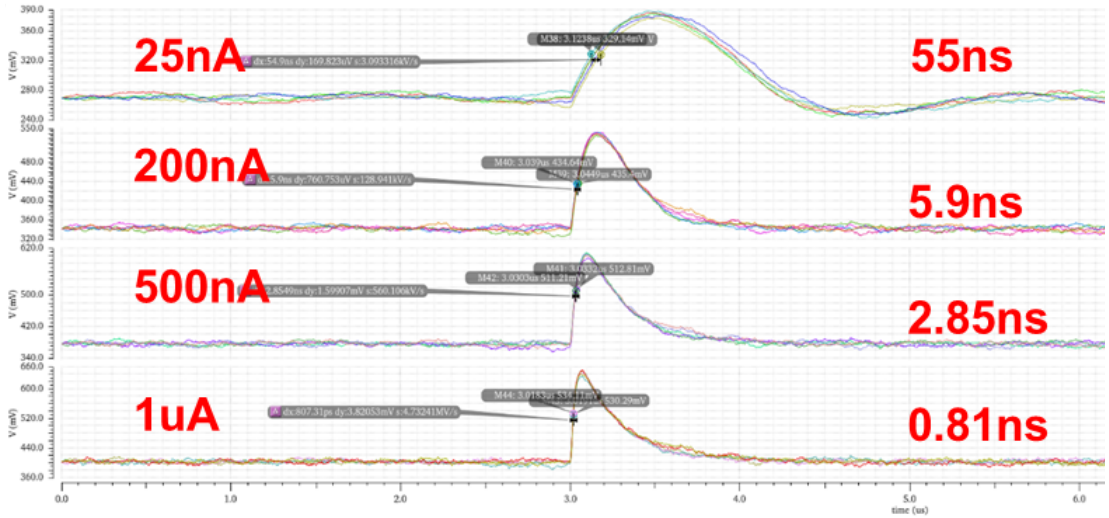
- Traditional FE architectures require methods to compensate for timewalk
  - **CFD** and **TOA/TOT calibration** (as in the TimePix chip) have been investigated



Timing jitter

- The effect of jitter affects the precision with which a signal edge is measured for a certain fixed charge
  - In the ALPIDE simulation model, the variation of hit response time with transient noise is 29 ns for the leading edge and 194 ns for the trailing edge

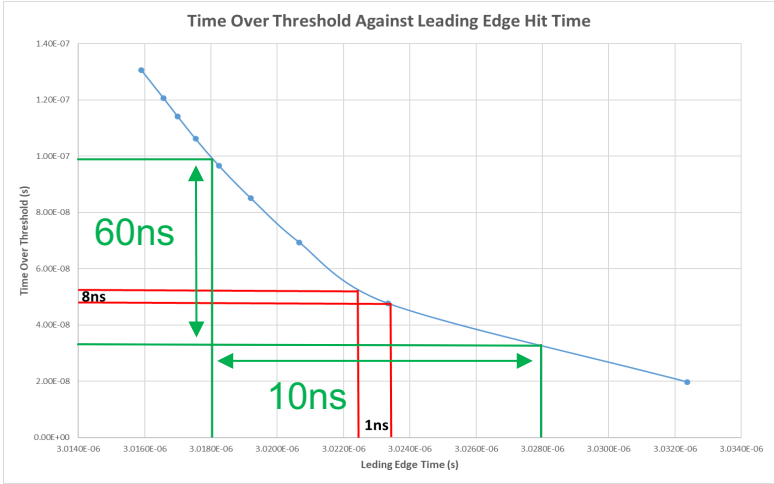
- Improving noise performance requires **higher power**



Transient noise simulation of a common source amplifier for different bias currents

TOT/TOA calibrated pixel

- Timewalk adjusted timing is obtained offline using TOA and TOT information
  - TOA and TOT need to measured with the required precision
- Transient noise simulations show that the noise performance of this architecture would be sufficient for the required time resolution
- However, this would be achieved only in a dedicated time stamping layer with a sensor different from the one used in vertex/tracker



Hit Size (e-)	ToA Standard Deviation (ps)	ToT Standard Deviation (ns)
500	429	2.45
750	278	3.21
2500	130	2.35

Pitch (μm)	Power Density (mW/cm^2)
20	4547
95	200
350	14.85

CFD pixel

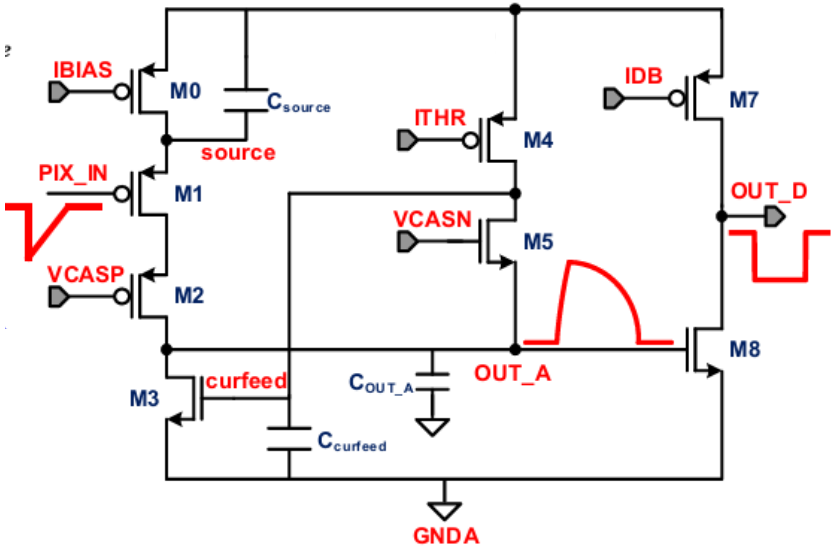
- Timewalk adjusted timing at pixel output (only TOA measurement is needed)
- Simulations of a CFD pixel architecture showed that a time resolution of 10 ns can be achieved also under the effect of noise
  - The simulated time-walk for charges between 0.5 and 2.5 ke- is around 3.6 ns
- The timing performance of this architecture is however significantly affected by **process variation**
  - Time-walk spread increases above 10 ns for some pixels
- Also in this case, a dedicated sensor would need to be designed for time stamping in an outer layer

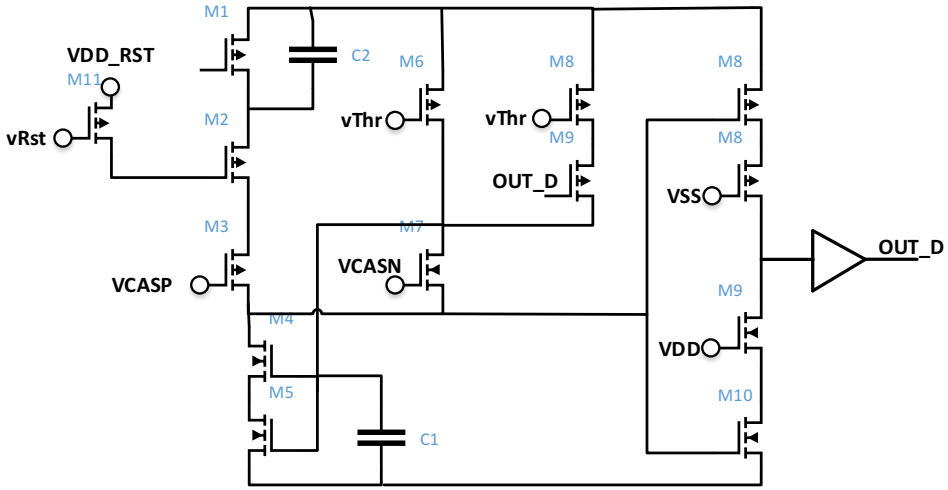
Pixel Pitch (μm)	Power Density (mW/cm^2)
20	2179
70	200
350	7.12

Low Power Front-End (LPFE)

- Strategy: design a **low power architecture** that meets the timing requirements for TOA/TOT measurement

- The ALPIDE design has been adapted to provide leading and trailing edges with timing jitter that meets our requirements
  - Adjustments to component sizes, cascoded inverter as the output stage, change to the **thresholding current mechanism**





LPFE precision on TOA & TOT measurement

- This architecture can meet the timing requirement for the leading edge at both the 10 ns and 1 ns specification
- In this architecture, the timing resolution depends on the signal amplitude
  - The smallest signal that can be detected will have a slower rising edge, so it will never achieve as good jitter as a larger signal

ToA Spread over 20 Transient Noise Runs		Signal Size		
		500 e-	750 e-	1000 e-
First Stage Bias Current	20 nA	48.3 ns	14.0 ns	5.86 ns
	40 nA	41.5 ns	7.8 ns	3.46 ns
	400 nA	27.4 ns	2.11 ns	0.92 ns

- Simulations show that the TOT can be measured with the required precision for the target TOA

LPFE power consumption

- With different bias currents, this architecture can meet both the 10 ns and the 1 ns timing requirements in a **20 µm pixel pitch**
  - The 10 ns requirement can be met for the required power density of the vertex and tracking detector (Q > 900 e-)
  - The 1 ns requirement can be met for the required power density of the timestamp layer (Q > 850 e-)

Front End Bias (nA)	Minimum Detectable Signal (e-)	Minimum 10 ns Resolution Signal (e-)	Minimum 1 ns Signal (e-)	Power Density per 20 µm pixel (mW/cm^2)
20	500	1000	N/A	9.7
40	500	900	N/A	19.1
400	500	750	850	150.7

Conclusion on feasibility study

- The LPFE design with TOT/TOA calibration shows promising features for the design of an EIC specific DMAPS sensor
  - Small improvements to the ALPIDE FE allow to design a sensor matching the EIC requirements, with added time stamping capability

- Despite the development of this sensor builds on the ALPIDE design, it will require significant resources from within the EIC (manpower and money) to deliver a detector for the EIC

- Is this the best way forward?

New baseline: ALICE ITS Upgrade in LS3 (ITS3)

- An alternative to an EIC specific detector development could be the ALICE ITS3

- See Leo Greiner's talk at the MIT meeting https://www.jlab.org/indico/event/348/session/5/material/0/0.pdf

- The ALICE ITS3 project aims at developing a **new generation MAPS** sensor with **extremely low mass** for the LHC Run4 (HL-LHC)

- It is very interesting for an EIC detector in many ways
  - Detector **specifications & timeline** compatible with those of the EIC
  - **Innovative development** suited to an EIC starting in approx. 10 years
  - **Large effort at CERN**
  - **Non-ALICE members welcomed** to contribute to the R&D to develop the technology for other applications

ALICE ITS3

Kickoff meeting held at CERN on December 4, 2019 for "ALICE ITS Upgrade in LS3"

https://indico.cern.ch/event/860914/

The most relevant efforts in this Letter of Intent (endorsed by the LHCC in September 2019) include:

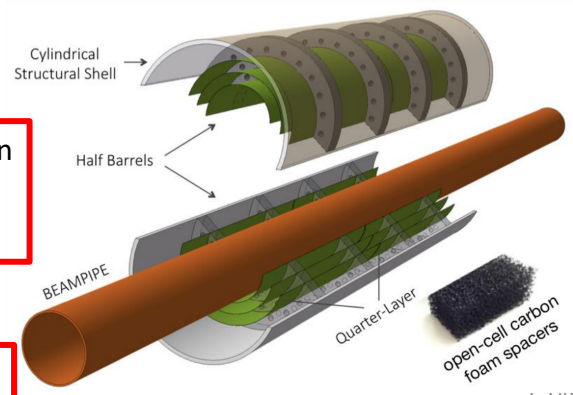
- Silicon R&D for next generation MAPS sensor (with significant improvements)

coupled with

- R&D into extremely low X/X0 cylindrical vertex detection with "bent" silicon

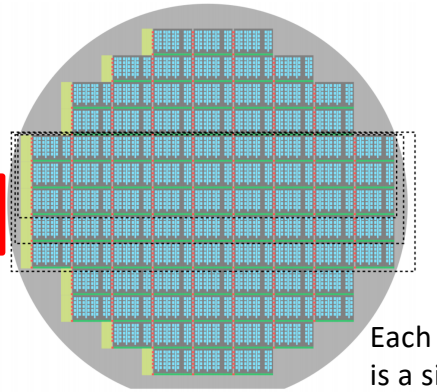
Much of this has already been presented by my colleague Vito Manzari at 2019 EIC User Group Meeting, 22-26 July 2019 Paris

"bent" silicon Detector concept



X/X0 ~ 0.05%

"stitched" silicon



Each layer half barrel is a single stitched sensor

ALICE ITS3 sensor

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

Next steps towards an ITS3 based EIC detector

- **Berkeley, Birmingham and RAL CMOS Sensor Group** are discussing the possibility of forming an EIC silicon vertex and tracking consortium to
  - Carry out coordinated work towards an ITS3 based EIC silicon vertex and tracking detector within the **EIC Generic Detector R&D programme**
    - A detailed proposal will be submitted to the panel in July
  - **Join the ITS3 R&D effort** as non-ALICE members to optimize the sensor characteristics (to the extent that they are not already) for use at the EIC
    - Face-to-face meeting with the ITS3 management at CERN to be scheduled in February

- To be able to join the ITS3 development within the next few months Birmingham would like to ask the committee to **re-purpose the remaining money allocated to the feasibility study** (approx. £25k), to switch designers' work to the **ITS3 pixel test vehicle submission** planned for Q3 2020

Conclusion and outlook

- eRD18 is bringing the **initial phase of the project to a close**
  - WP1 technology investigations have been completed and reported
  - WP1 feasibility study on pixel FE design has been completed
  - WP2 basic detector layout simulations have been completed
  - Reports for the feasibility study and basic layout simulations are being finalised

- The **second phase** of the project will be carried out in collaboration with Berkeley and RAL CMOS Sensor Group and will cover
  - Work on **ITS3 technology** to design the EIC silicon vertex and tracking detector
  - **Heavy flavour physics simulations** to inform the Detector/Physics Working Group input into the EIC Detector Yellow Report

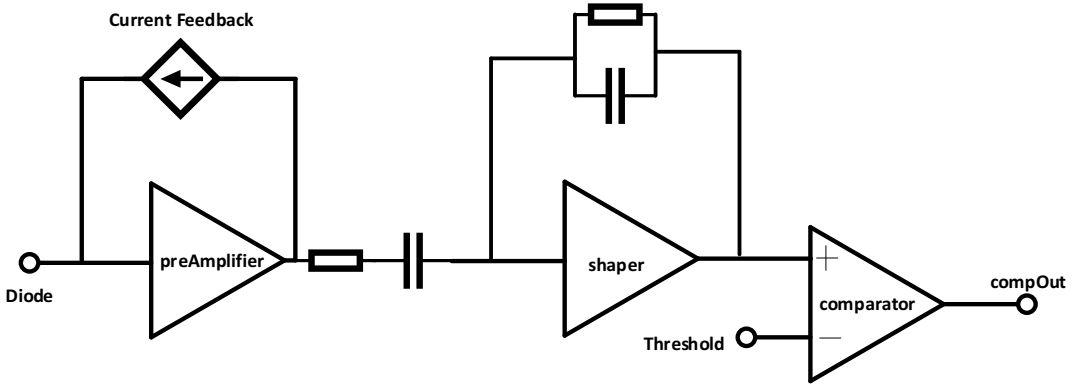
Backup

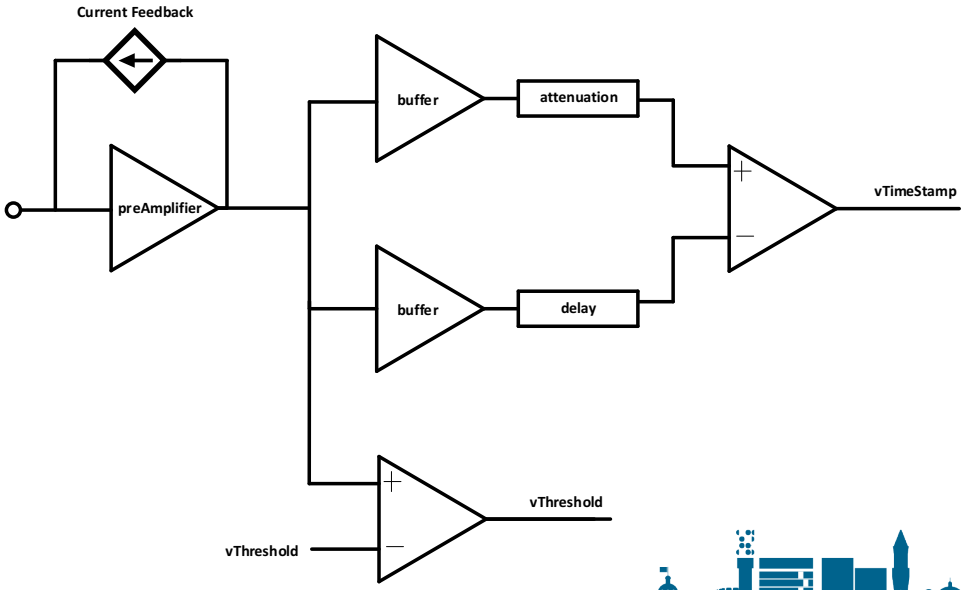
Time-walk correction methods

- TOA/TOT calibration (as in TimePix3)
  - Little additional circuitry required, FE would be very similar to ALPIDE
  - Calibration procedure needed
  - Timewalk adjusted timing obtained offline
  - ToA and ToT data must both be read out

- Constant fraction discriminator
  - Timewalk adjusted timing is direct output of pixel
  - Only ToA data needs to be read out
  - Complex pixel design

Calibrated pixel & CFD pixel schematics





ALPIDE FE with higher bias current

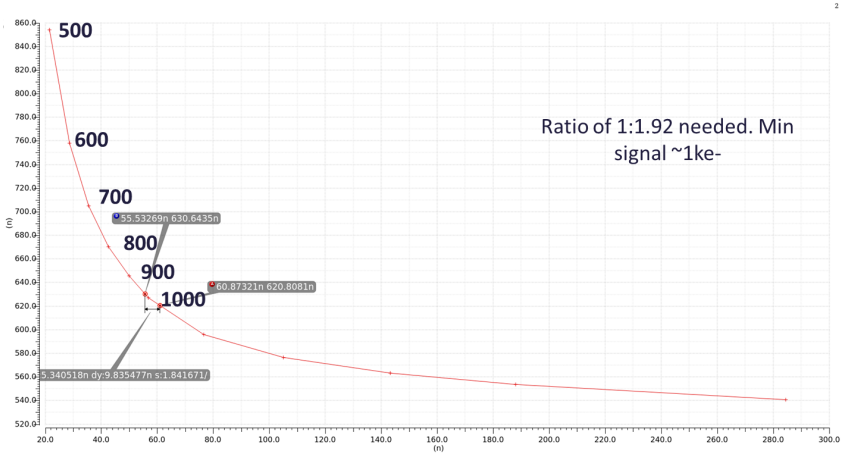
- With higher bias current the ALPIDE can reach 10 ns time resolution
- Using ALPIDE in this mode ToT can be as long as 5 μs for a 2.5 ke- signal and a high bias current
  - The clipping diode has been removed to allow TOT measurement
  - This would be too long for the 2 μs target integration time

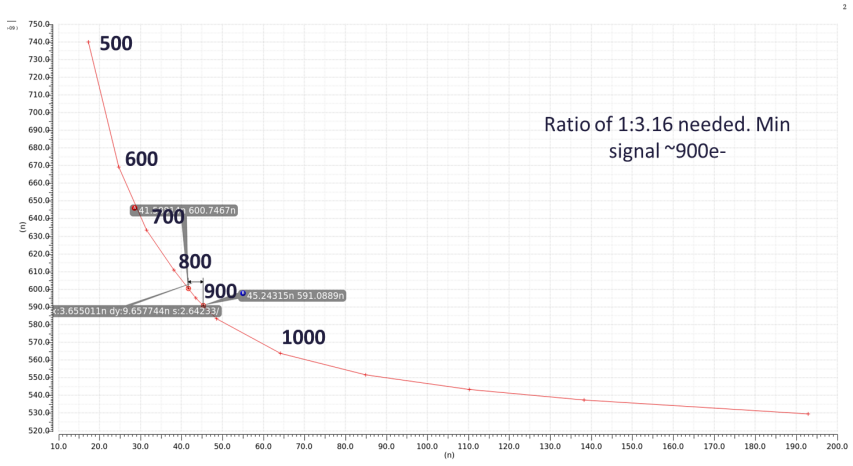
ToA Spread over 20 Transient Noise Runs		Signal Size		
		500 e-	750 e-	1000 e-
First Stage Bias Current	20 nA	127 ns	33.4 ns	16.1 ns
	40 nA	121 ns	20.9 ns	8.92 ns
	400 nA	91.2 ns	4.4 ns	1.55 ns

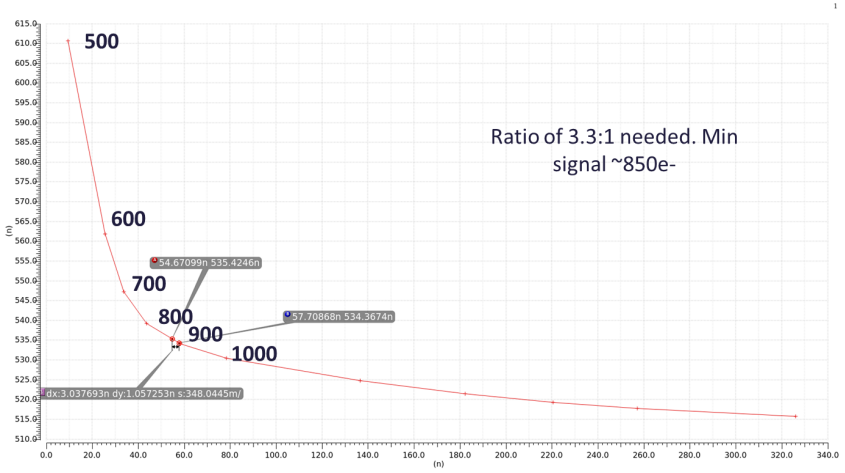
Power (mW/cm^2)		First Stage Bias Current (A)		
		20 nA	40 nA	400 nA
Pitch	20 μm	16.2	27.2	121.5
	350 μm	0.053	0.089	0.397

LPFE precision on TOT measurement

ToT Spread over 20 Transient Noise Runs (ns)		Signal Size		
		500	750	1000
First Stage Bias Current (A)	20n	4.95	4.45	5.19 (1:1.92)
	40n	3.90	4.42 (1:2.26)	3.16 (1:3.16)
	400n	4.8	2.03 (1:4.93)	3.3 (3.3:1)







Transient run simulations of LPFE

- Recorded ToA across 500 transient noise runs for a bias current of 400nA and three different hit sizes - 500e- (green), 750e- (blue) and 1000e- (pink)